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APPLICATION NO.	FILING DATE .	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/582,897	06/13/2006	Masanori Akita	TR-US065126	4958
22919 7590 09/13/2007 GLOBAL IP COUNSELORS, LLP			EXAMINER	
	REET, NW, SUITE 700		SOON, SHELDON STEWART	
WASHINGTO	ON, DC 20036-2680		ART UNIT	PAPER NUMBER
			2841	
	,		MAIL DATE	DELIVERY MODE
			09/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
	10/582,897	AKITA ET AL.				
Office Action Summary	Examiner	Art Unit				
	Sheldon S. Soon	2841				
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet wi	th the correspondence address				
A SHORTENED STATUTORY PERIOD FOR REF WHICHEVER IS LONGER, FROM THE MAILING Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailting date of this communication. If NO period for reply is specified above, the maximum statutory perions are reply within the set or extended period for reply will, by state that the period for reply will be stated by the period for reply wil	DATE OF THIS COMMUNIC 1.136(a). In no event, however, may a not od will apply and will expire SIX (6) MON ute, cause the application to become AB	CATION. eply be timely filed ITHS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).				
Status		·				
1) Responsive to communication(s) filed on 21	November 2006.					
,	•					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice unde	r <i>Ex parte Quayle</i> , 1935 C.D	. 11, 453 O.G. 213.				
Disposition of Claims						
4) Claim(s) <u>1-5</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-5</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and	i/or election requirement.					
Application Papers						
9)☐ The specification is objected to by the Exami	ner.					
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.						
Applicant may not request that any objection to the						
Replacement drawing sheet(s) including the corr						
11)☐ The oath or declaration is objected to by the	Examiner. Note the attached	Office Action of form PTO-152.				
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for forei	gn priority under 35 U.S.C. §	119(a)-(d) or (f).				
1.⊠ Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the pr		received in this National Stage				
application from the International Bure						
* See the attached detailed Office action for a li	ist of the certified copies not	received.				
•						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)		Summary (PTO-413) s)/Mail Date				
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date DOD.		nformal Patent Application				

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DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Iketani (US PG Pub 2002/0004250).

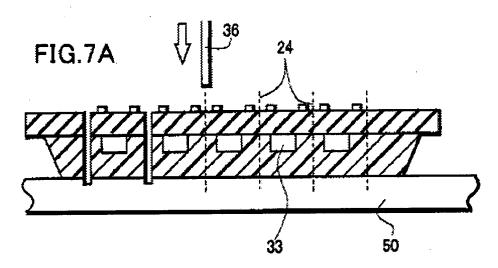


Figure 7A from Iketani

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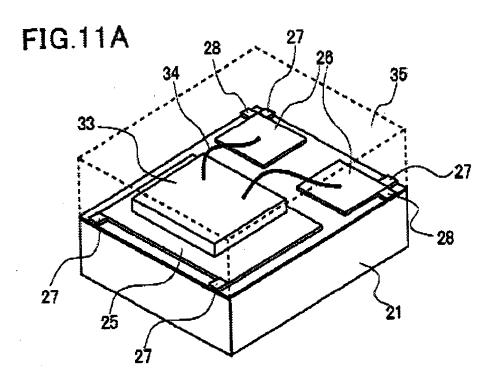
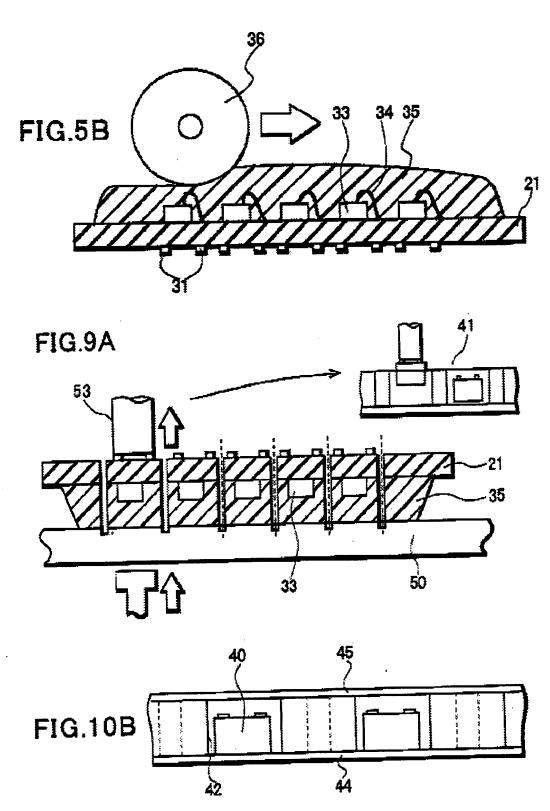


Figure 11A from Iketani

Regarding Claim 1 – Iketani discloses all the elements of the instant invention including: a plurality of good interposer boards (item 21); and a carrier tape (item 50) being formed an exfoliate layer,

the good interposer boards being disposed on the carrier tape at every predetermined interval, the good interposer board having a base member (items 25 and 26) mounting an IC chip (item 33), extended electrodes (item 26) being formed on the base member each being connected to corresponding a electrode of the IC chip (items 34), and an adhesive laver being formed to cover the extended electrode (item 35). The examiner takes official notice that in the fabrication process, items 25 and 26 are formed as one piece and later cut.

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Figures 5B, 9A and 10B from Iketani

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00.44

Regarding Claim 2 – Iketani discloses all the elements of the method including: applying adhesive (resin, item 35) on extended electrodes (item 34) of an interposer board tape (item 21), the interposer board tape being obtained by forming the extended electrodes (items 26) on a base member (items 25 and 26), a plurality of IC chips (items 33) being mounted on the base member, and each of the extended electrodes (items 34) being connected to corresponding electrode of each of the IC chips; obtaining individual interposer boards by cutting (as shown in figure 7A) the interposer board tape, and selecting only good interposer boards (as explained in paragraph 0058); and

disposing only the interposer boards on a carrier tape (as shown in figure 9A) at every predetermined interval, the carrier tape being obtained by forming an exfoliate layer (item 45) on a base tape (item 44).

Regarding Claim 3 – Iketani discloses all the elements of the method including: first means (the method shown in figure 5B) for applying adhesive (item 35) on extended electrodes (item 26) of an interposer board tape (item 21), the interposer board tape being obtained by forming the extended electrodes on a base member (item 25 and 26), a plurality of IC chips (items 33) being mounted on the base member, and each of the extended electrodes being connected to corresponding electrode of each of the IC chips;

second means for obtaining individual interposer boards by cutting the interposer board tape (as shown in figure 7A);

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third means for selecting only good interposer boards(as explained in paragraph 0058); and

fourth means for disposing only the interposer boards on a carrier tape (as shown in figure 9A) at every predetermined interval, the carrier tape being obtained by forming an exfoliate layer (item 45) on a base tape (item 44).

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emori et al (US Patent 6,378,774) herein referred to as Emori in view of Iketani.

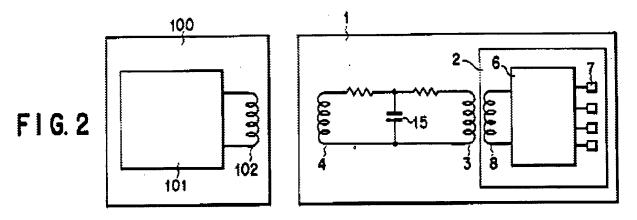


Figure 2 from Emori

Regarding Claim 4 – Emori discloses the elements of depressing (the abstract discloses, The IC module has both a contact-type function and a non-contact-type function) the interposer board (smart card, item 1) to an antenna circuit board tape (item 101) to face antenna electrodes (item 102) formed on an antenna circuit base material

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film (item 100) and the extended electrodes, but fails to disclose: peeling an interposer board from an electronic circuit board intermediate member, the electronic circuit board intermediate member being obtained by disposing interposer boards on a carrier tape at every predetermined interval, the interposer board being obtained by mounting an IC chip, by forming extended electrodes each connected to a corresponding electrode of the IC chip, and by forming an adhesive layer to cover the extended electrodes, the carrier tape being obtained by forming an exfoliate layer on one face of a base tape. Iketani teaches forming a circuit comprising: peeling an interposer board (item 21) from an electronic circuit board intermediate member (item of figure 10B), the electronic circuit board intermediate member being obtained by disposing interposer boards (items 40) on a carrier tape (as shown in figure 9A) at every predetermined interval, the interposer board being obtained by mounting an IC chip (item 33), by forming extended electrodes (items 26) each connected to a corresponding electrode of the IC chip (item 34), and by forming an adhesive layer (item 35) to cover the extended electrodes, the carrier tape being obtained by forming an exfoliate layer (item 45) on one face of a base tape (item 44). It would have been obvious to someone skilled in the art at the time of the invention to construct the IC module of Emori with the semiconductor circuit of Iketani since Iketani states in the first paragraph that Iketani's semiconductor device uses a smaller mounting area without lead forming at considerable reduction of manufacturing cost.

Regarding Claim 5 – Emori discloses a means for depressing (the abstract discloses, The IC module has both a contact-type function and a non-contact-type function) the

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interposer board (smart card, item 1) to an antenna circuit board tape (item 101) to face antenna electrodes (item 102) formed on an antenna circuit base material film and the extended electrodes (item 100), but fails to disclose, a means for peeling an interposer board one by one from an electronic circuit board intermediate member, the electronic circuit board intermediate member being obtained by disposing interposer boards on a carrier tape at every predetermined interval, each interposer board being obtained by mounting an IC chip, by forming extended electrodes each connected to corresponding electrode of the IC chip, and by forming an adhesive layer to cover the extended electrodes, the carrier tape being obtained by forming an exfoliate layer on one face of a base tape.

Iketani teaches: a means for peeling an interposer board one by one from an electronic circuit board intermediate member (as shown in figure 9A), the electronic circuit board intermediate member being obtained by disposing interposer boards (items 40) on a carrier tape (as shown in figure 9A) at every predetermined interval, each interposer board being obtained by mounting an IC chip (item 33), by forming extended electrodes (items 26) each connected to corresponding electrode of the IC chip (item 34), and by forming an adhesive layer (item 35) to cover the extended electrodes, the carrier tape being obtained by forming an exfoliate layer (item 45) on one face of a base tape (item 44).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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Iketani

US PG Pub 2002/0019066

Pendse

US Patent 5,768,776

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheldon S. Soon whose telephone number is 571-272-9092. The examiner can normally be reached on Monday through Friday 8:30-5:00 est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on 571-272-2800, ex. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TUAN T. DINH PRIMARY EXAMINER Sheldon S Soon Examiner Art Unit 2841